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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,422	08/30/2000	Jeffrey W. Honeycutt	M122-1332	9935

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EXAMINER

KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 02/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/651,422

Applicant(s)

HONEYCUTT ET AL.

Examiner

Jennifer M. Kennedy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

Applicant's election of Group II, claims 1-20, in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

Claim 20 is objected to because of the following informalities: Line 2 of claim 20 contains a spelling error. The examiner believes that "to" should be changed to "two". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al. (U.S. Patent No. 5,700,349) in view of Parekh et al. (U.S. Patent No. 5,918,122).

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Tsukamoto et al. disclose the method of forming an insulative material along a conductive structure, comprising, providing a conductive structure (5) over a substrate (1), forming an electrically insulative material (9) along at least a portion of the conductive structure, the electrically insulative material comprising at least one of $\text{Si}_x\text{O}_y\text{N}_z$ and Al_pO_q (see column 4, lines 40-50, and column 9, 24-34) wherein p, q, x, y, and z are greater than 0 and less than 10, and forming a doped oxide material (10) of BPSG over the insulative material.

Tsukamoto et al. also discloses the method wherein the electrically insulative material is $\text{Si}_x\text{O}_y\text{N}_z$ or Al_pO_q and is against the conductive structure,

Tsukamoto et al. do not disclose the method of forming a dopant barrier layer over the electrically insulative material. Parekh et al. disclose the method of forming a dopant barrier layer (24) over an electrically insulative material (30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer over the electrically insulative material, as Parekh et al. teaches (see column 1, lines 40-45), in order to inhibit diffusion of the phosphorous from the BPSG layer into the underlying materials.

Tsukamoto et al. and Parekh et al. do not disclose the method wherein the insulative material is formed to a thickness of at least 50 angstroms. It would have been obvious matter of design choice to form the structure having the claimed ranges of thickness since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. In re Daily, 93 USPQ 47 (CCPA

1966), the court held that changes in size and shape of parts of an invention in the absence of an unexpected result involves routine skill in the art. Additionally, In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. (U.S. Patent No. 6,245,669).

Fu et al. disclose the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (14) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (22, 24) along at least a portion of the conductive structure, the electrically insulative material comprising at least two separate layers, the at least two layer having different chemical compositions from one another, a first of the two layer comprising at least one of $\text{Si}_x\text{O}_y\text{N}_z$ and Al_pO_q wherein p, q, x, y, and z are greater than 0 and less than 10, the second of the at least two layer consisting essentially of silicon and nitrogen.

Fu et al. do not explicitly disclose the method of anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall. The

examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform anisotropic process to form the spacers on the sidewall of the gate. Anisotropic etching processes are well known and used in the art because they allow the formation of a thin layer of insulation or fine feature patterning.

Fu et al. do not explicitly disclose the method wherein the spacer is used to align the dopant during the implant. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the spacers to align during dopant implantation. The use of spacers for aligning during and implantation is well known and used in the art to prevent misalignment.

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. (U.S. Patent No. 6,245,669).

Fu et al. disclose the method substantially as claimed, and rejected above, but do not disclose the method wherein the first of the at least two layer is between the second of the at least two layer and the transistor, or the method wherein the first of the at least two layers is Al_pO_q . Tsukamoto et al. disclose the method wherein an insulative material of silicon nitride can be replaced with $\text{Si}_x\text{O}_y\text{N}_z$ or Al_pO_q (see column 4, lines 40-

50 and column 9, lines 24-34) with the same basic desired effects. Thus, Tsukamoto et al. teaches that the silicon nitride and the silicon oxynitride are functional equivalents. While Fu teaches a sequential silicon nitride, silicon oxynitride spacer, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacer of Fu et al. with silicon oxynitride and silicon nitride, respectively since silicon nitride and silicon oxynitride are recognized as functional equivalents in the art and would result in the same basic desired effects. Similarly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the spacer of Fu et al. with aluminum oxide and silicon nitride respectively, since silicon nitride, silicon oxynitride and aluminum oxide are recognized as functional equivalents in the art and would result in the same basic desired effects.

Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto et al. (U.S. Patent No. 5,700,349) in view of Parekh et al. (U.S. Patent No. 5,918,122).

Tsukamoto et al. disclose the method of forming a transistor structure, comprising, forming a transistor gate (5) over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material, forming source/drain regions (8) within the substrate and proximate the transistor gate, forming an electrically insulative material (9) along a conductive structure of the transistor gate sidewall, the electrically insulative material comprising at least one of $\text{Si}_x\text{O}_y\text{N}_z$ and Al_pO_q (see column

4, lines 40-50, and column 9, 24-34) wherein p, q, x, y, and z are greater than 0 and less than 10, and forming a doped oxide material (10) of BPSG over the insulative material.

Tsukamoto et al. do not disclose the method of forming a dopant barrier layer over the electrically insulative material by chemically vapor depositing silicon oxide utilizing an TEOS precursor. Parekh et al. disclose the method of forming a dopant barrier layer (24) over an electrically insulative material (30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer over the electrically insulative material, as Parekh et al. teaches (see column 1, lines 40-45), in order to inhibit diffusion of the phosphorous from the BPSG layer into the underlying materials.

Tsukamoto and Parekh et al. do not explicitly disclose the method wherein the oxide layer is formed by a CVD deposition with TEOS as the precursor. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide layer of Parekh et al. with a CVD method and TEOS as the precursor. Silicon oxide layers are commonly formed with a CVD method in which TEOS is used as the precursor to provide an oxide layer with excellent conformality.

Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. (U.S. Patent No. 6,245,669).

Fu et al. disclose the method of forming transistor structure, comprising, forming a transistor gate over a substrate, the transistor gate (14) comprising a sidewall which comprises electrically conductive material, forming an electrically insulative material (22, 24) along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprises two different layer that are against one another, one of the layers consisting of silicon nitride, and the other of the two layers consisting of either at least one of $\text{Si}_x\text{O}_y\text{N}_z$ and Al_pO_q wherein p, q, x, y, and z are greater than 0 and less than 10.

Fu et al. do not explicitly disclose the method of anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform anisotropic process to form the spacers on the sidewall of the gate. Anisotropic etching processes are well known and used in the art because they allow the formation of a thin layer of insulation or fine feature patterning.

Fu et al. do not explicitly disclose the method wherein the spacer is used to align the dopant during the implant. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-

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known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the spacers to align during dopant implantation. The use of spacers for aligning during and implantation is well known and used in the art to prevent misalignment.

Fu et al. do not disclose the method of forming a dopant barrier layer over the electrically insulative material. Parekh et al. disclose the method of forming a dopant barrier layer (24) over an electrically insulative material (30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dopant barrier layer over the electrically insulative material, as Parekh et al. teaches (see column 1, lines 40-45), in order to inhibit diffusion of the phosphorous from the BPSG layer into the underlying materials.

Fu and Parekh et al. do not explicitly disclose the method wherein the oxide layer is formed by a CVD deposition with TEOS as the precursor. The examiner takes official notice of facts outside the record which are capable of instant and unquestionable demonstration as being "well-known" in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxide layer of Parekh et al. with a CVD method and TEOS as the precursor. Silicon oxide layers are commonly formed with a CVD method in which TEOS is used as the precursor to provide an oxide layer with excellent conformality.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (703) 308-6171. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

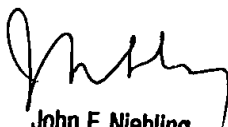
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Jmk

January 28, 2002


John F. Niebling
Supervisory Patent Examiner
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